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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/915,160	07/25/2001	Toshiharu Yanagida	09792909-5171	7228

7590 06/01/2004

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/915,160	YANAGIDA, TOSHIHARU	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,5,6 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2, 5, 6 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 5, 6 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. (US 6,333,206), hereafter Ito, in view of Nishikawa et al. (US 5,878,943), hereafter Nishikawa, and Milewski et al. (US 6,330,967), hereafter Milewski and Andros et al. (US 5,633,533), hereafter Andros.

Regarding claims 2, 5, 6 and 25, Figure 28 of Ito shows a semiconductor apparatus comprising: a semiconductor chip 3 inherently having a circuit pattern; a plurality of solder bumps 2 of two different materials on the semiconductor chip connect to the circuit pattern, the solder bumps forming spaces; a resin film 10 disposed on the semiconductor chip and said solder bumps, said resin film being disposed in the spaces between solder bumps such that upper surfaces of said solder bumps protrude from said resin layer; and a mounting board 1.

Regarding the aspect of the solder ball having a eutectic solder layer disposed on the surface of the solder ball, starting on column 5, lines 29, Ito shows a variety of materials for solder balls. In particular, Ito discloses a gold-plated bump with a copper or nickel core, indicating eutectic material (gold) on the outer surface of the solder ball.

Ito does not teach a precoated solder layer on the land. Figure 4 of Milewski teaches a solder layer 51 (Cu layer with an oxidation inhibitor on the surface) on the lands 53 (col. 5, lines

1-5) aligned with the solder bumps on the mounting board 21. It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Milewski in to the device of Ito in order to have a solder layer on the lands to enhance the attachment of chips to a mounting board.

The combined teaching of Ito and Milewski fail to show the aspect of cleaning the metal bumps. Figure 18 of Nishikawa shows in the surfaces of the metal bumps being cleaned (col.12, lines 18-25). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Nishikawa to the device of Ito and Milewski in order to enhance the strength of the soldered junction through having a clean surface of metal bumps.

The device with combined teachings of Ito, Milewski and Nishikawa is substantially identical except a gap formation between the resin layer and the mounting board. Figure 6 of Andros shows a semiconductor device with a gap formation between the resin layer (51; col.5, lines 25-27) and the board (27). It would have been obvious to one of ordinary skill in the art to modify the layer of the resin formation in the device of Ito, Milewski and Nishikawa with the teaching of Andros for the protection of the semiconductor device only.

In addition, a different embodiment (Figure 13) of Ito also shows spacing between a resin formation (18 or 13 on the chip) and the board (13).

Regarding claim 2, Nishikawa teaches the surfaces of the metal bumps being cleaned of components causing a rise of a connection resistance and a drop in a joint strength at least connection interfaces. Nishikawa teaches, throughout the specification especially in col. 1, lines 22-40, cleaning method of oxide/contamination coating on the surface of metal bumps to enhance better alignment between the soldering joint.

Response to Arguments

Applicant's arguments filed March 18, 2004 have been fully considered but they are not persuasive. The rejection still stands.

Starting on page 5, line 2, Applicant argues that "Milewski *teaches away* from the use of such precoated land *and* a coated solder ball." First, Examiner would like to point out that the instant invention recites a limitation of "a precoated *solder layer* disposed *on the lands*. the Office Action above discusses this aspect in detail with the teachings of Milewski.

And Applicant further argues "the technology of Andros is quite different from and incompatible with the technologies of Ito, Nishikawa, Milewski, and the present invention." However, the instant invention is regarding a device and a patentable weight is carried on a device structure regardless of how the device is made. As discussed in the office action, Andros is referred only to show a gap formation in a semiconductor device is known in the art.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

ORI NADAV
patent examiner